Critical Assessment of Substrate and Mask Blank Readiness

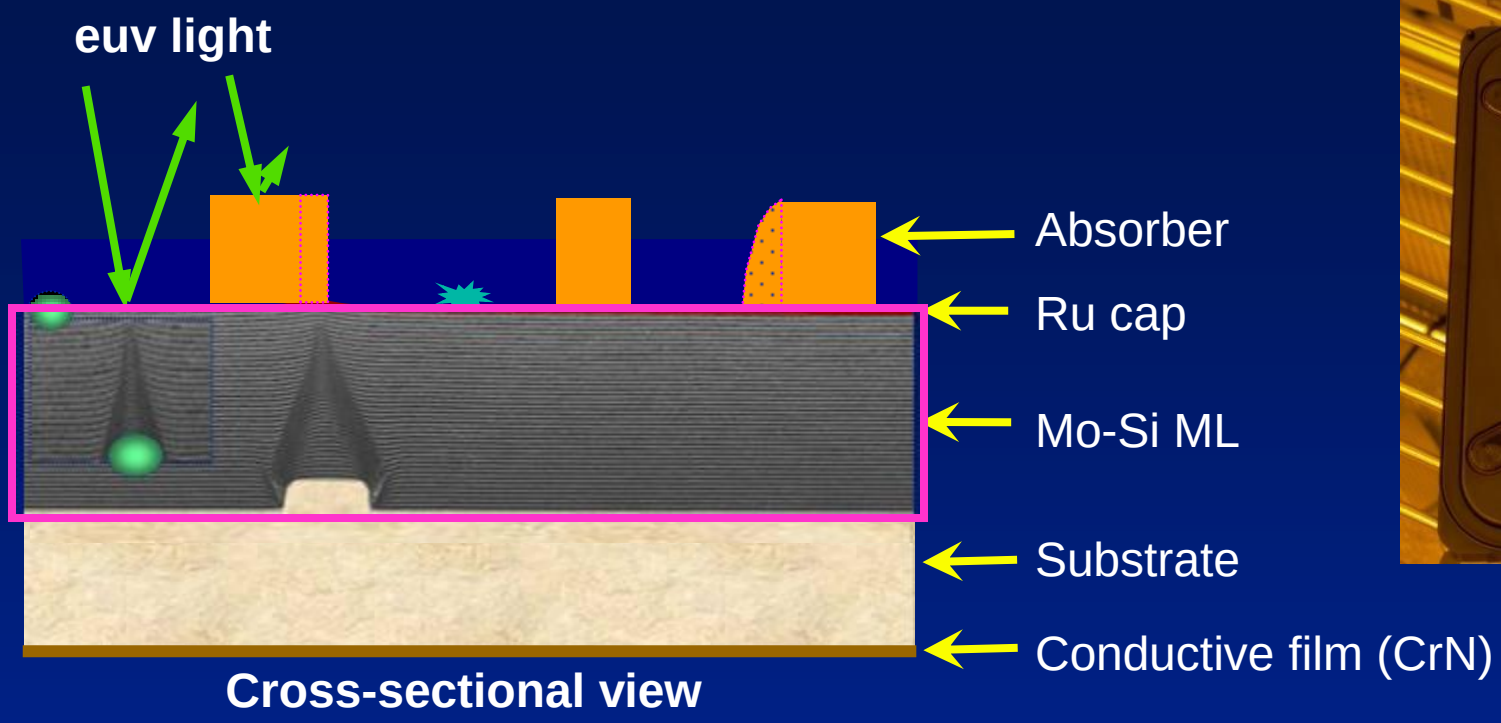
Ted Liang
Pei-yang Yan, Guojing Zhang,
John Magana, Seh-Jin Park, Firoz Ghadiali
Gilroy Vandentop, Rajesh Nagpal

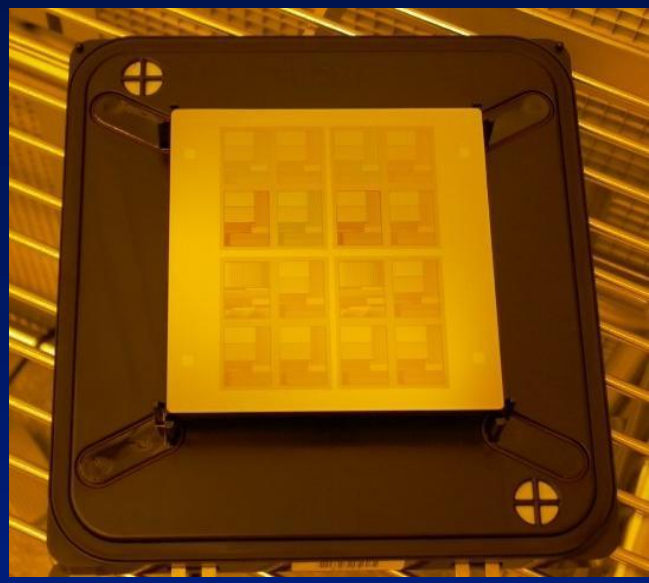
Intel Corporation

→ **Unbiased overview … from users' point of view**

→ **Intel's most complete understanding of …**

Intricacy of an EUV mask





- **EUV mask yield is <u>all</u> (almost) about ML stack**
  - Defects
  - Layer roughness
  - Durability against irradiation, use and cleans
- **There will be defect in a blank; can it be used?**

Pragmatic

~~Critical~~ Assessment of ML Blank Readiness

- Requirement and Infrastructure -

Pragmatic: Dealing with things sensibly and realistically in a way that is based on practical rather than theoretical considerations

Vs.

Critical: expressing or involving an analysis of the merits and faults of …

A Measure of Readiness

- **Two scenarios, all must be affordable:**
  - Ideal: blank quality = 193nm optical blanks; EUV mask yield is simpler
  - Painful = blank is defective: mitigation methodology & infrastructure must be ready
- **If quality blanks not ready when needed, then we ask:**
  - **what is limiting the rate of progress?**
    - fundamental engineering know-how's?
    - infrastructure availability?
    - validity of the requirements as currently understood?
- **Industry must address these questions collectively to enable mask yield**
- **This presentation is to review and analyze the status and 'prognosis', and discuss what need to be done to get ready**
  - Intel integrated approach
  - NOT let mask be the limiter to EUV lithography realization

Outline

- Blank quality
- Current defect status, understanding
- Defect Requirements
- Infrastructure needs and readiness
- Summary

Total Blank Quality

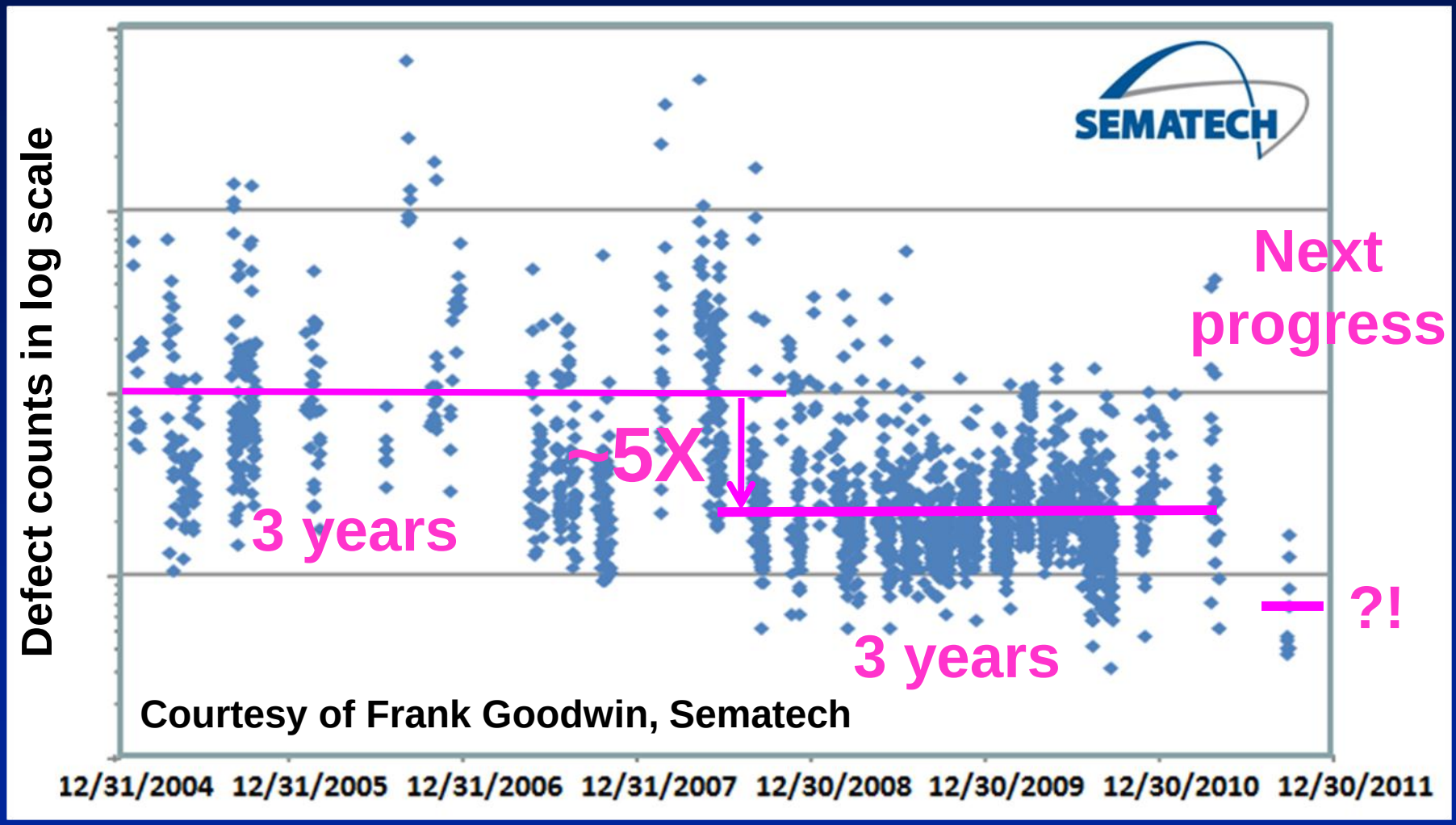
- **ML blanks**
  - Flatness
  - Defect
  - Surface/stack roughness
  - Fiducial mark quality
  - Maintenance/storage before absorber deposition
  - ……
- **Absorber blanks**
  - Similar quality to 193nm blanks
  - Absorber stack thickness

Outline

- Introduction: blank quality
- **Current defect status, understanding**
- Defect Requirements
- Infrastructure needs and readiness
- Summary

Historical Sematech Experimentations

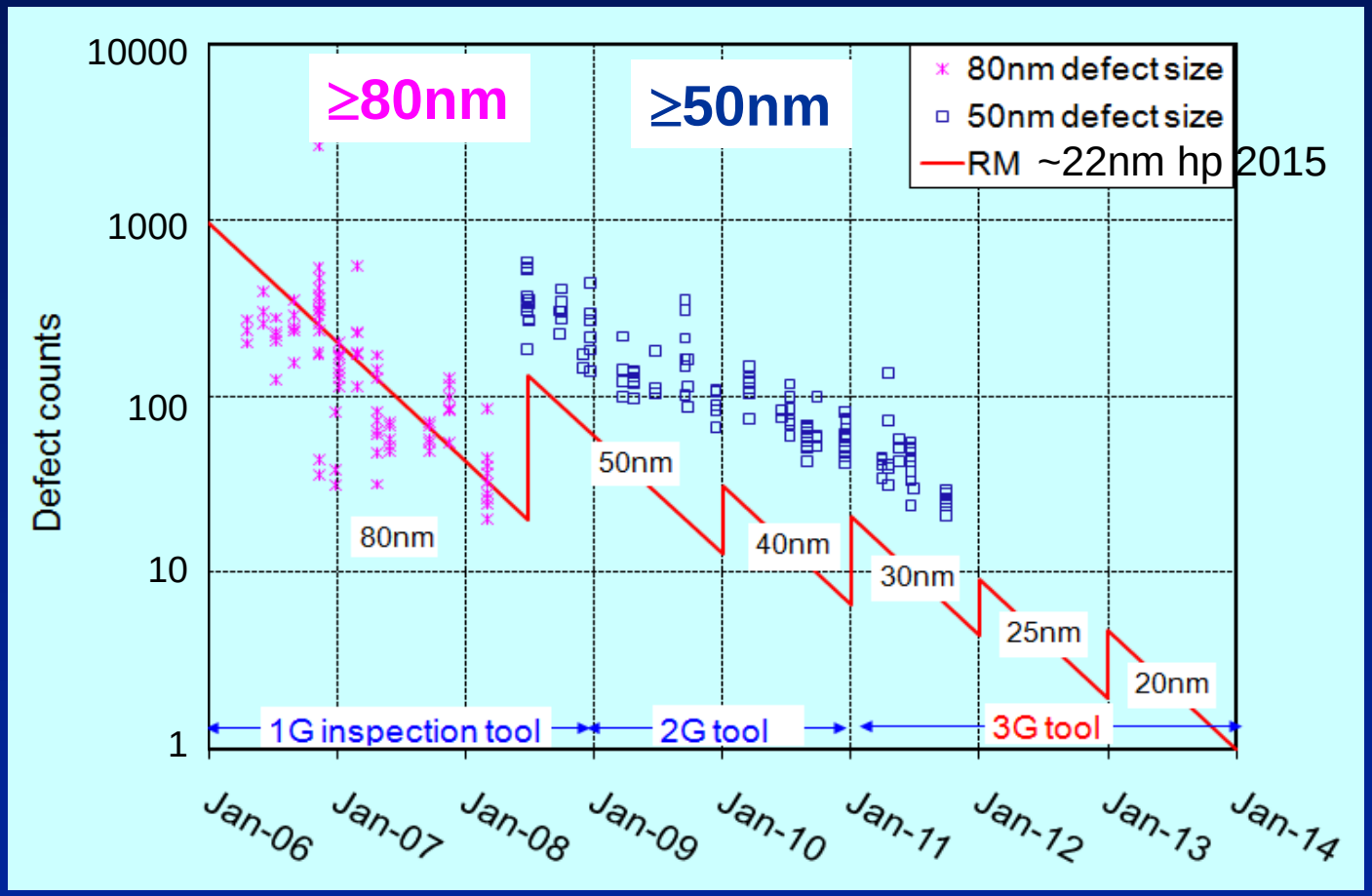
- Represents ML blank defect reduction by trial and error

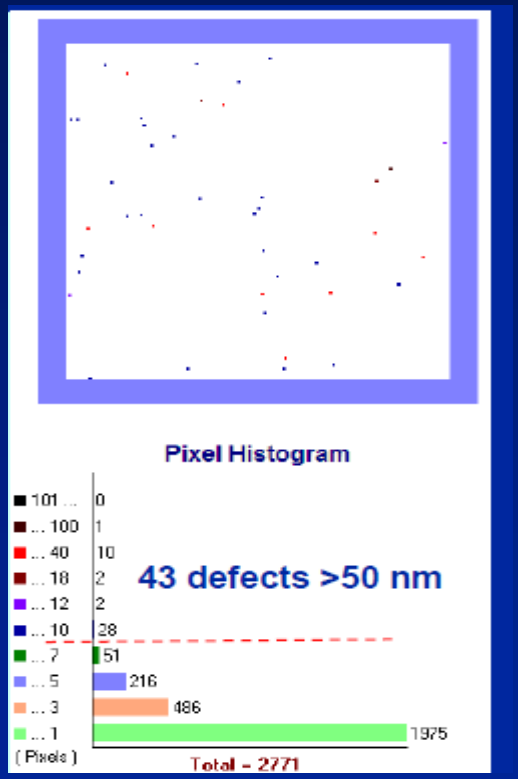


- Wide distribution, different exploratory tests
  - Need stable, well controlled process → production worthy

Historical Defect Trend – Commercial Blanks

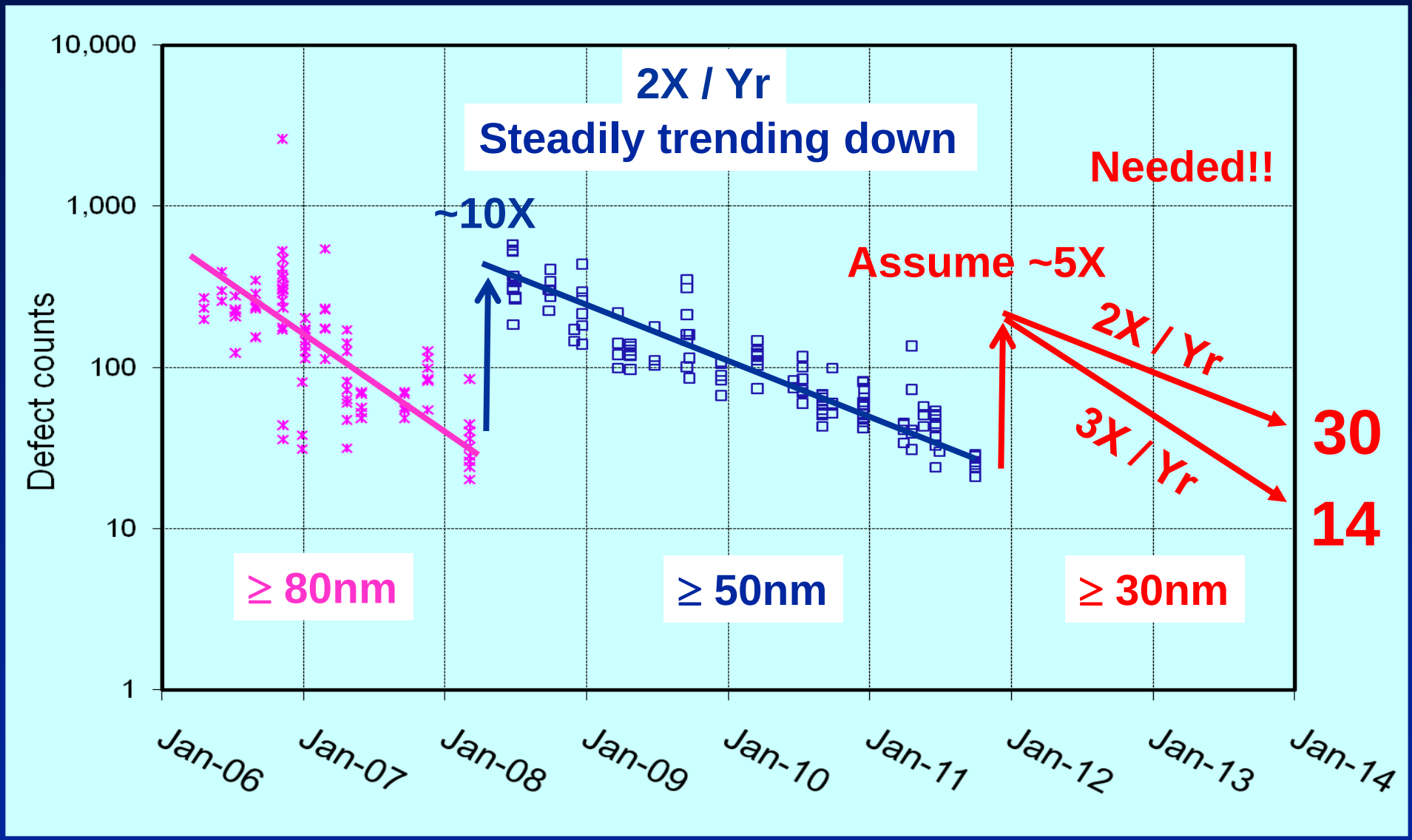
- Steady reduction in total defect count





A typical quality blank

Need to Maintain Reduction Trend for Smaller Defects



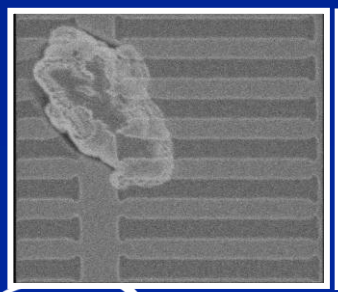
- Looking into the details – size, tools, requirements
- ***Focus on blank yield***

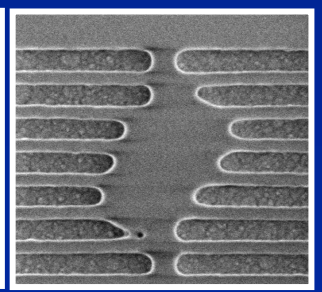
ML Defect Partition, Impact

- Total # not a complete description of blank yield
- Defect size matters: partition into different size bins based on impact to mask yield, printability
- Different origins; different solutions
  - Handling; deposition process
  - substrate

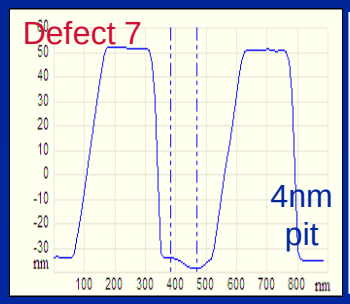
Bin	Relative Size	Impact	Goal : Solution
Large	> hp	Killer	Elimination
Medium	≈ hp to ½ hp	Killer to ΔCD	Elimination + reduction : Mitigation
Small	≈ < ½ hp	ΔCD	Reduction : Compensation

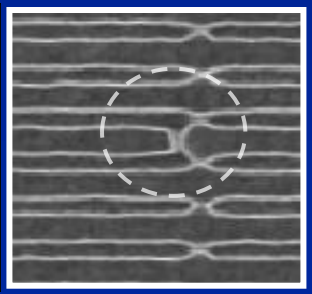
L



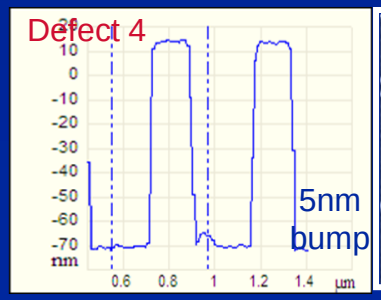


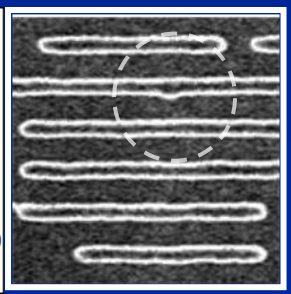
M





S

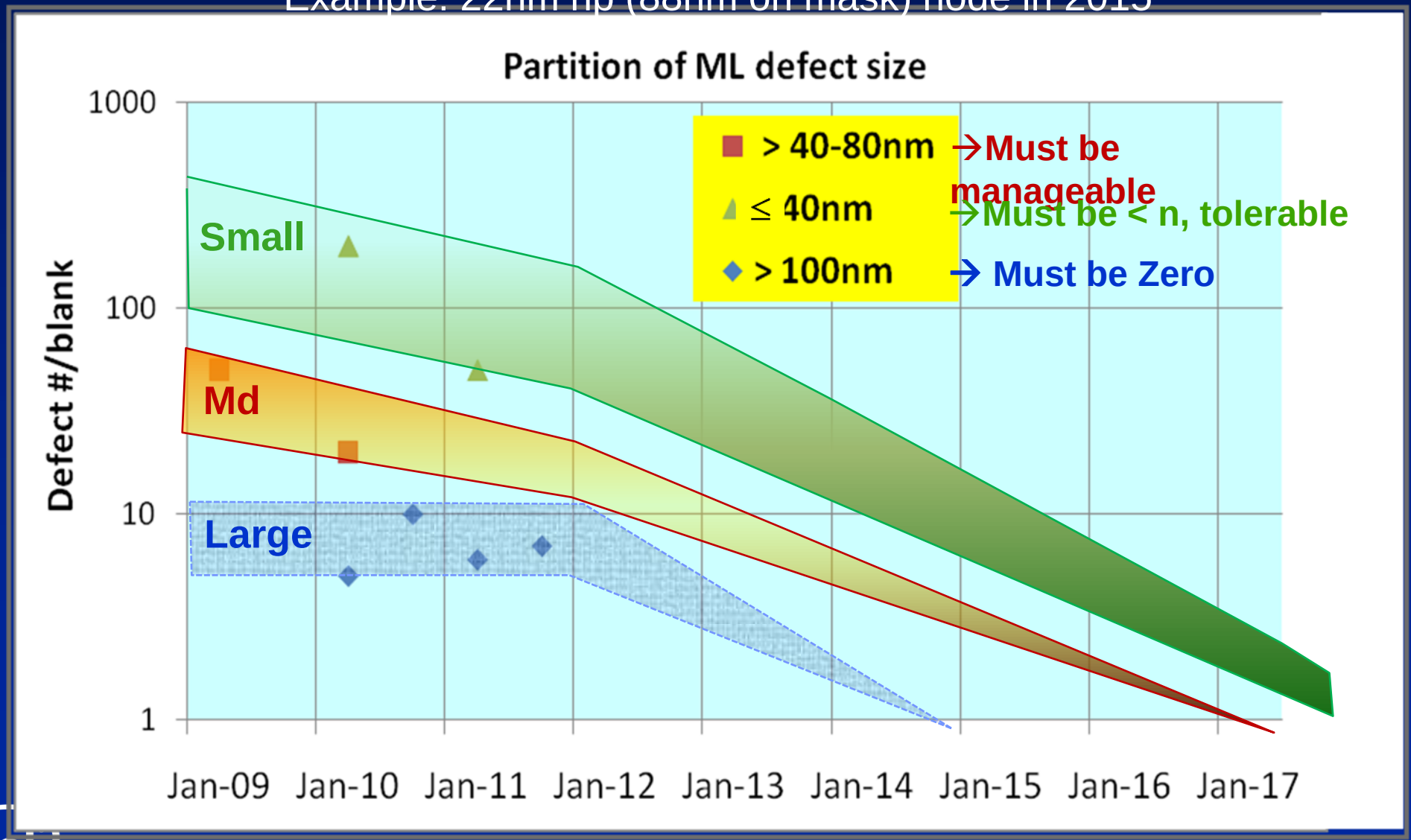




Hypothesizing the Blank Defect Goal

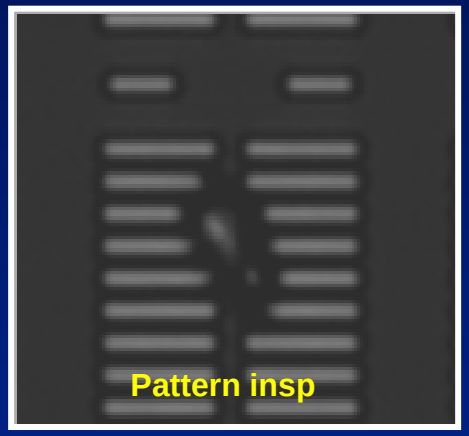
- Manage size and # to achieve mask yield
- Rate of reduction needs to be accelerated

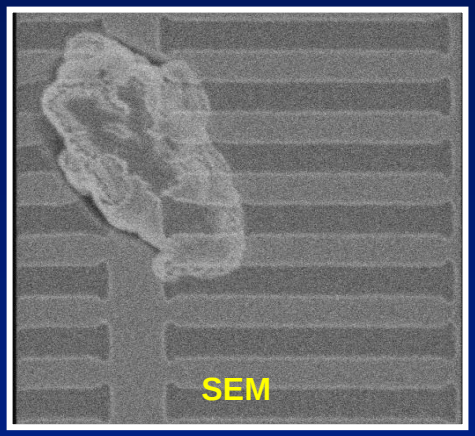
Example: 22nm hp (88nm on mask) node in 2015

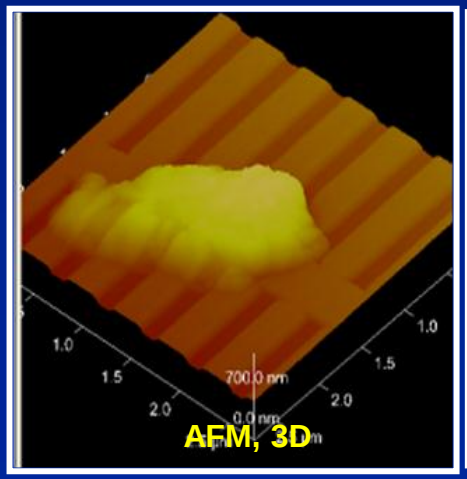


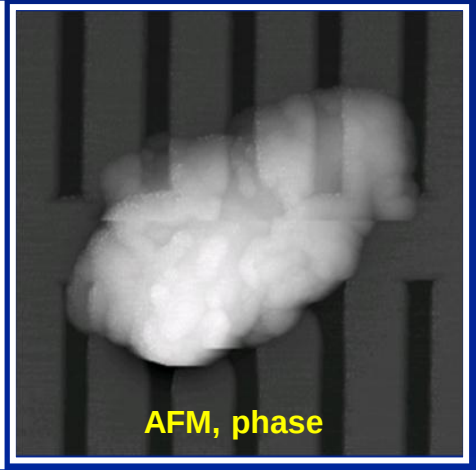
#1 Concern: Large Defects

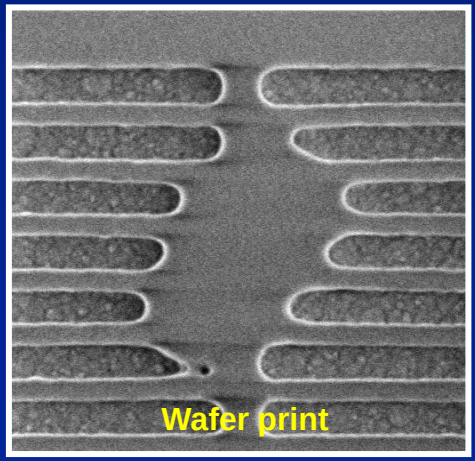
- **Size >> hp, cause line to bridge**
  - Can not hide under primary patterns
  - Can not be compensated (repaired) – print even when isolated









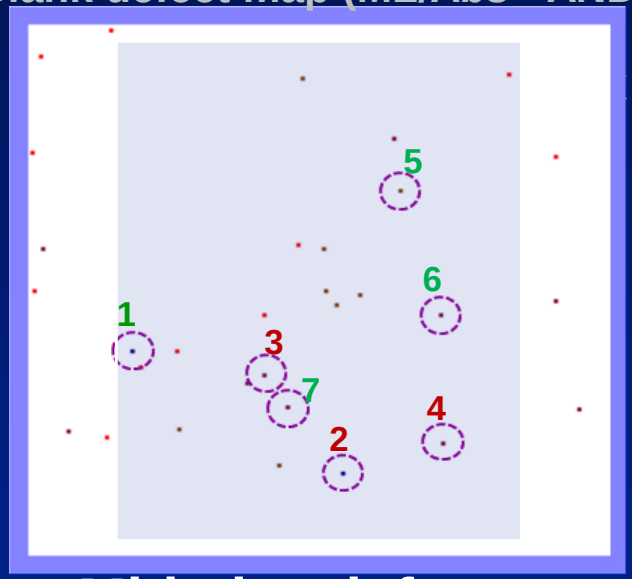


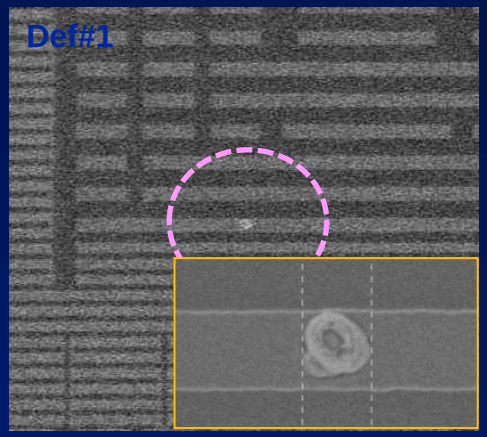
- **Impact: mask yield = 0**

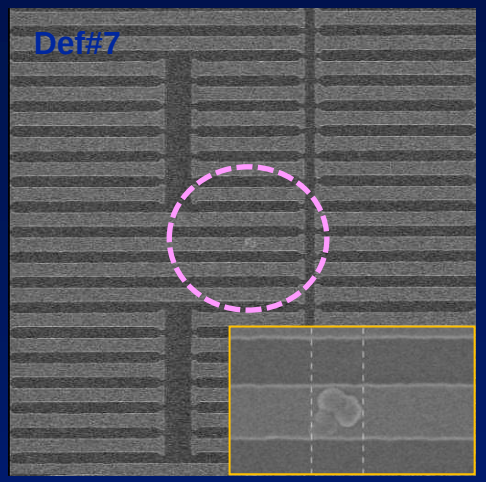
Large Defects Limit Mitigation Success

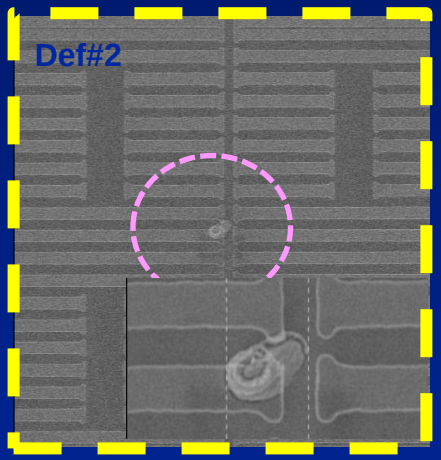
7 ML defect mitigated on an 22nm device, but
incomplete due to a large defect
(1 defect covered with no pattern shift)

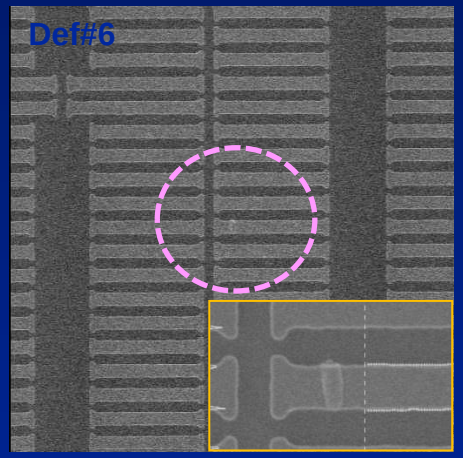
Blank defect map (ML/Abs –AND)



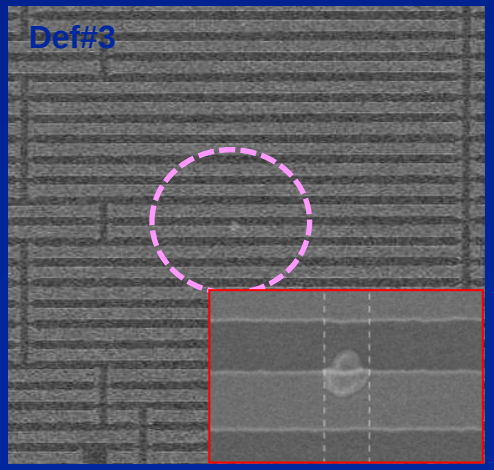


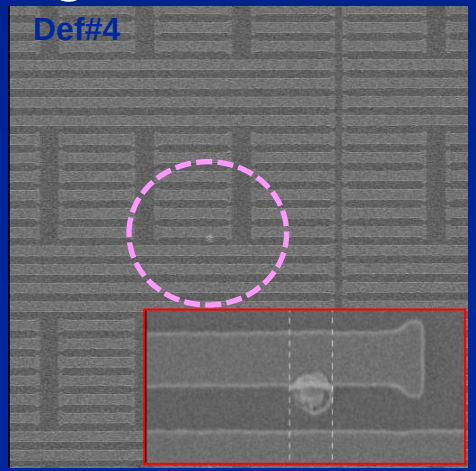


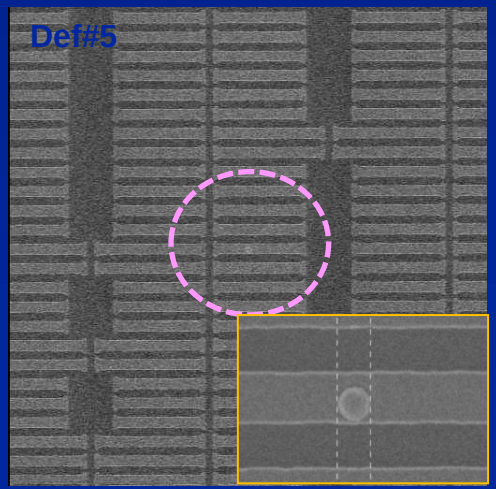




Mid-size defects mitigation successful



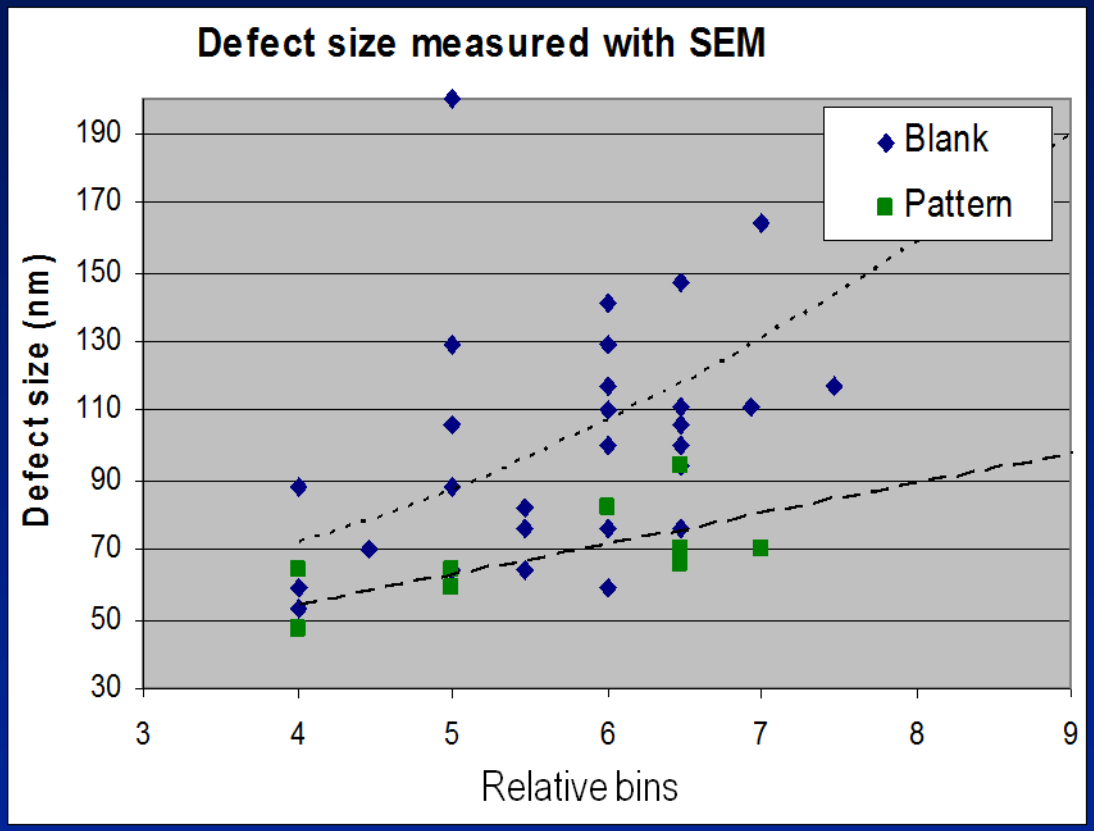


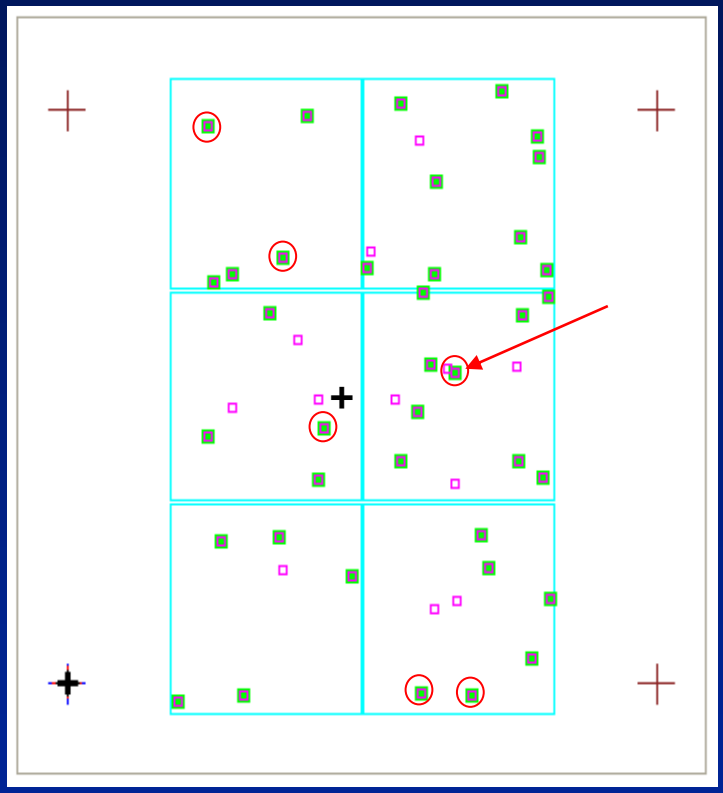


G. Zhang et al: 2010 EUVS

Large Defects Must Be Eliminated

- **Many large defects are <u>amplitude-like</u>**
  - Visible to SEM and pattern inspection





- **<u>Defect source</u> must be eliminated**
  - Handling of substrate before coating
  - 'Fall-on', flaking, during ML coating
  - Targets

Small ML Defects

- **Sizes: ≈< ½ hp of primary mask patterns**
- **Origins**
  - Substrate defects: pits, bumps, ML decoration
  - Most are phase defects
- **Impact**
  - Not every defect prints
  - Most can be compensated by absorber alteration
- **Density must be reduced to acceptable level**
  - Tolerant level depends on device layer and pattern density
  - Recent reduction trend promising

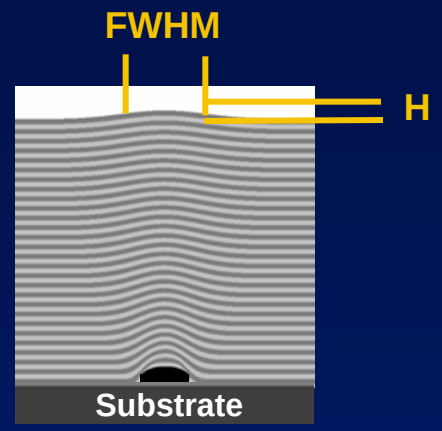
All Things Considered:

What size of the smallest defects we care about
and
how many can be tolerated?

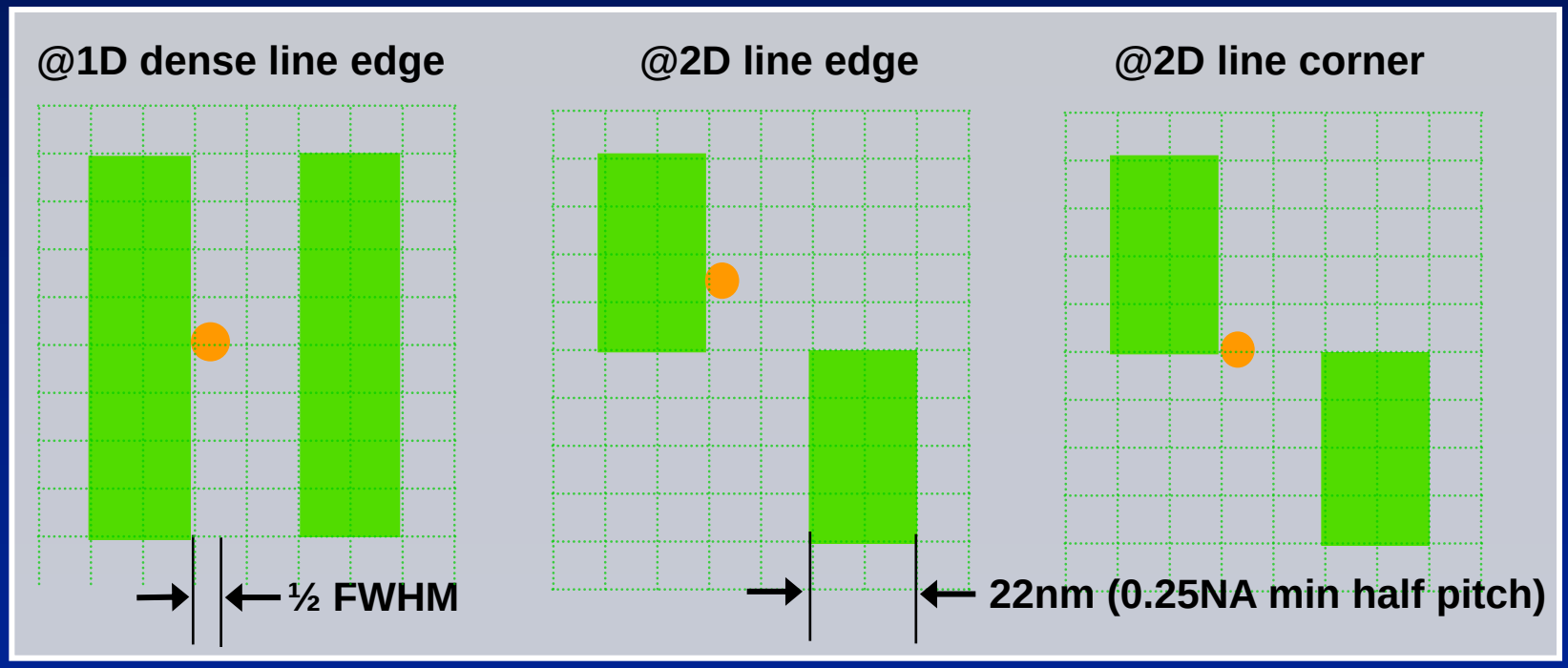
Outline

- Introduction: blank quality
- Current defect status, understanding
- **Defect Requirements**
- Infrastructure needs and readiness
- Summary

Defect Printability by Simulations



- **Min. printable defect for three cases near 22nm lines**
- **Printability is sensitive to bump height and location**
  - Worse location is about ½ (FWHM) from absorber pattern line edge



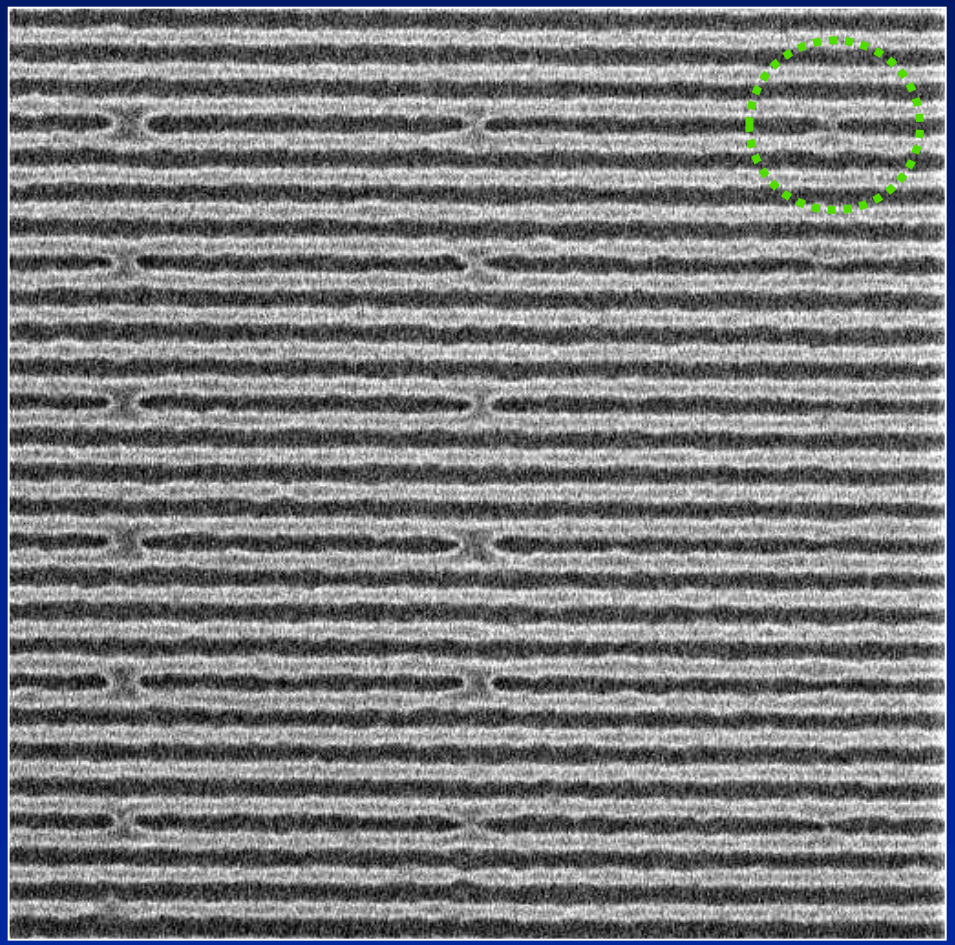
- **Printable height of 60nm wide phase bump from aerial image simulations**

10% ΔCD	1nm	2.5nm	2.5nm
20% ΔCD	1.5nm	3.5nm	3.0nm

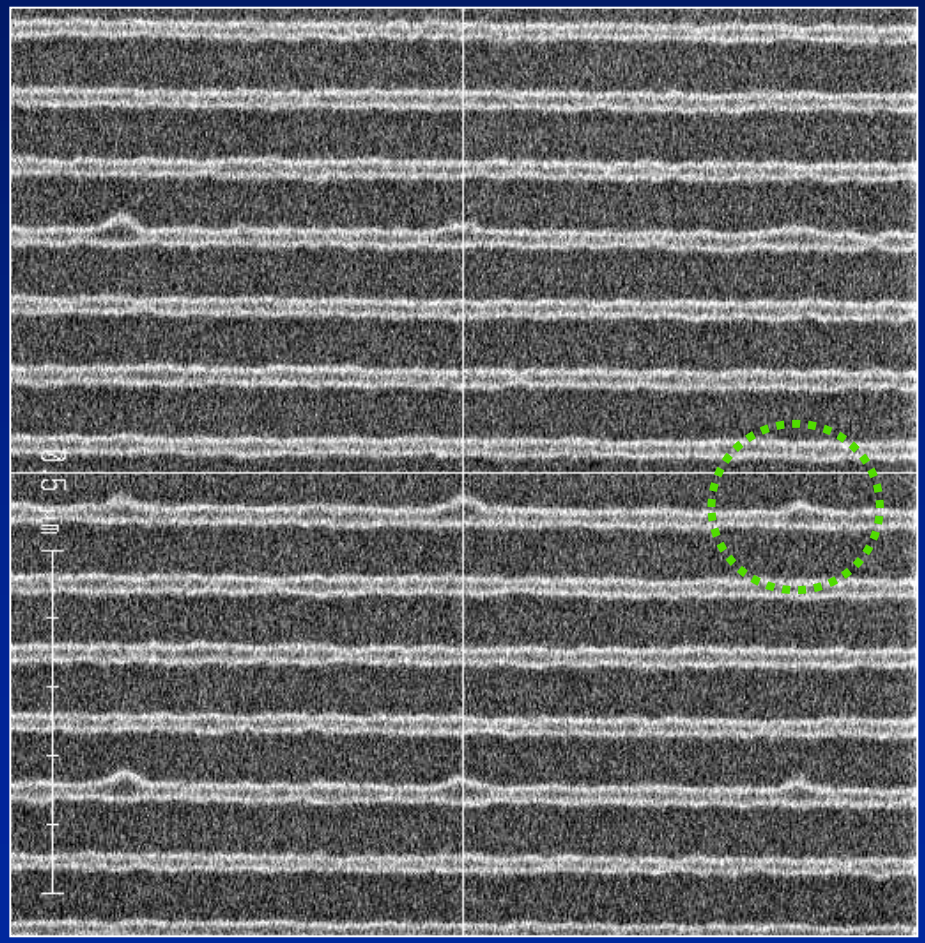
Printability by Resist Prints

- Printability of programmed ML defects
- 2nm ML phase bump for 25nm resist lines

Caused line bridge
25nm 1:1 LS



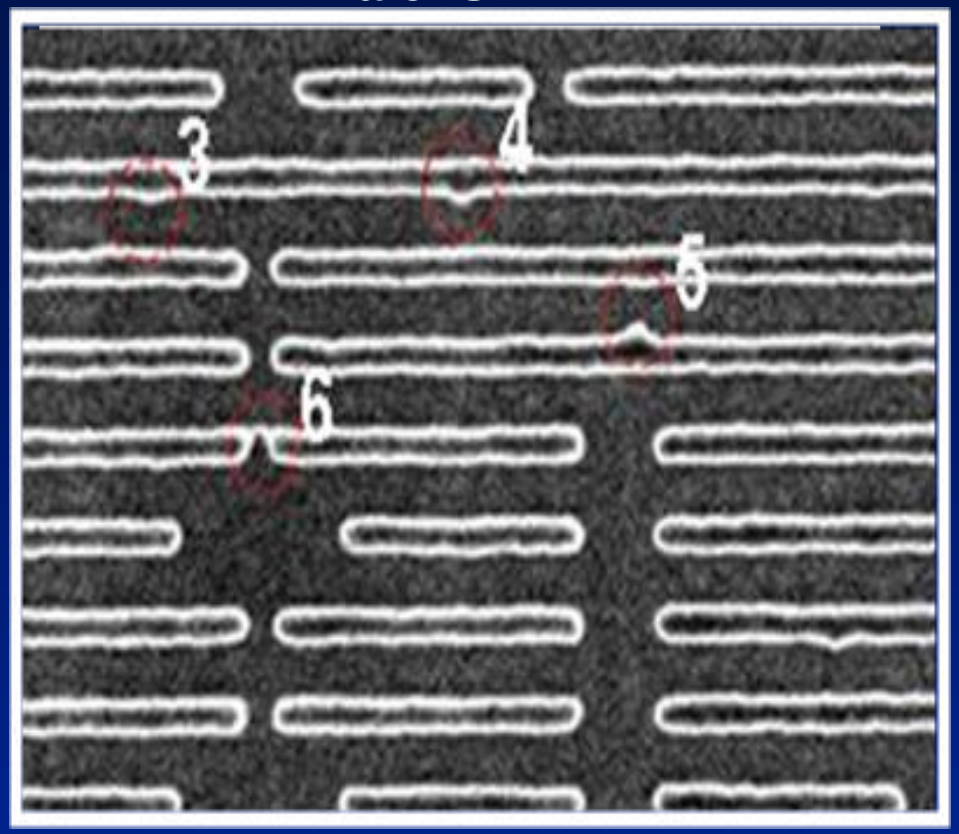
Caused 20% ΔCD
25nm 1:3 LS



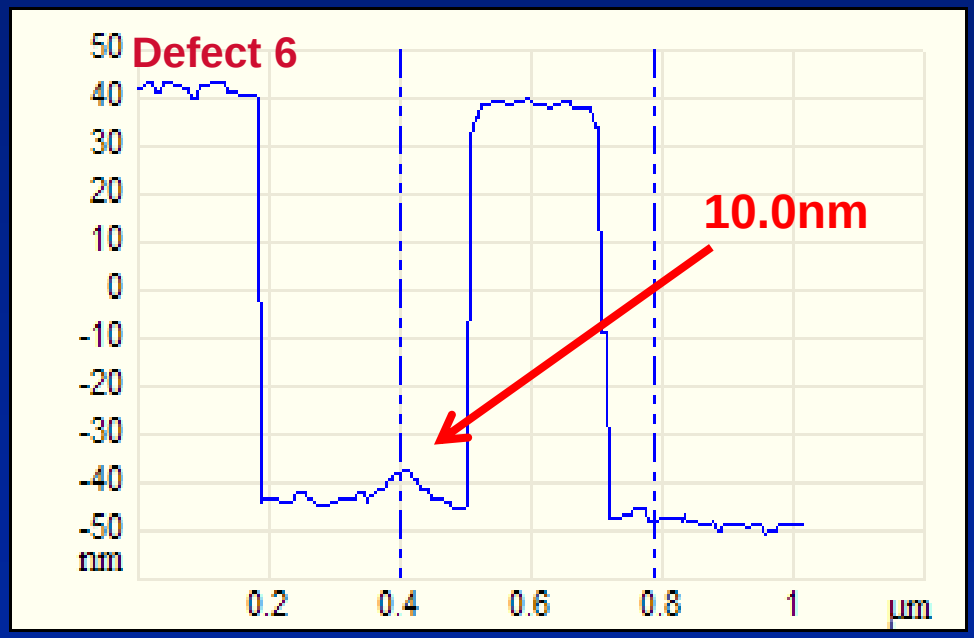
Grant Kloster, Intel

Printability of Defects on a Commercial Blank

Wafer SEM



AFM scan on a finished mask



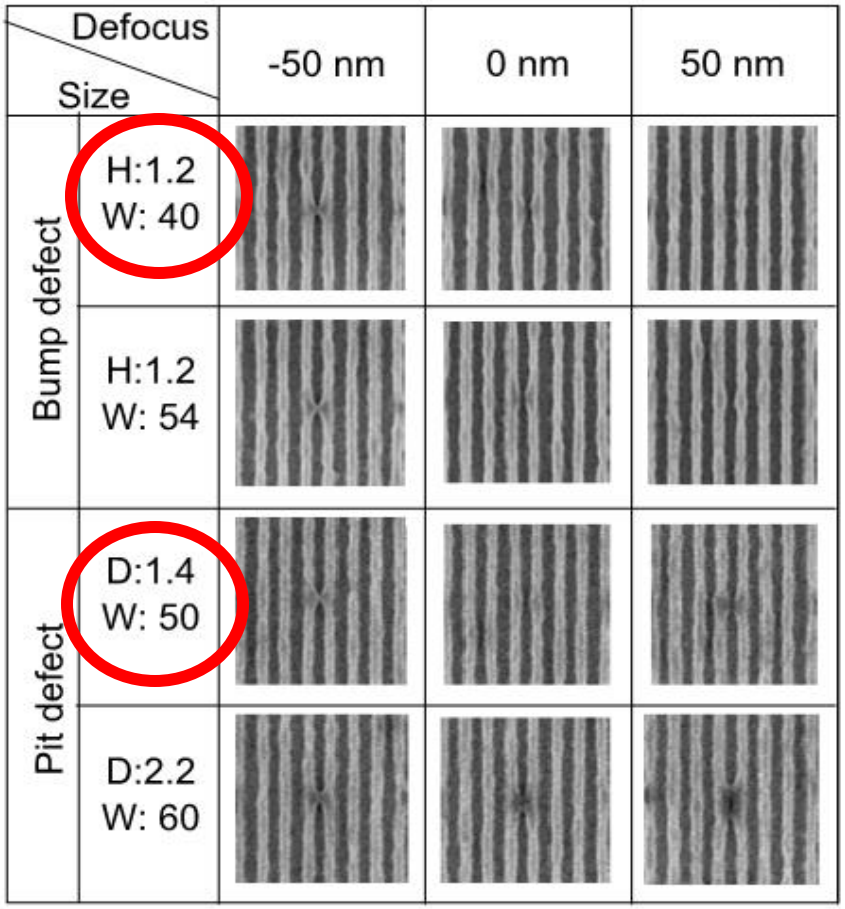
- Must reduce such cluster of ML defects
- Limit the number of repair sites

J. Magana et al, 2010 BACUS

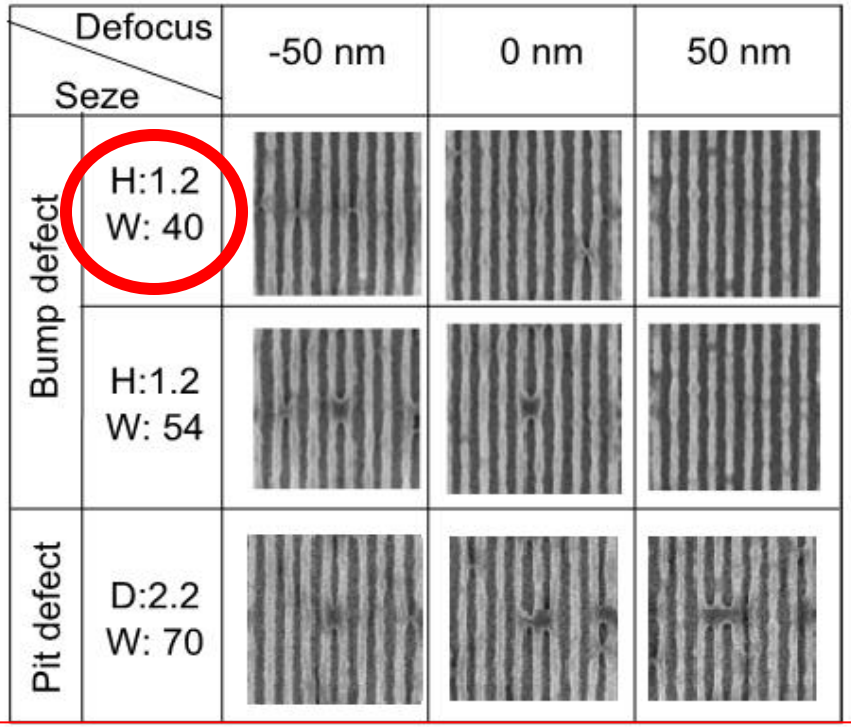
Printability by Resist Prints (cont'd)

IRAI Phase defect impact on 26nm, 24 nm patterns Selete

26 nm L/S patterns



24 nm L/S patterns



- L:S the most defect sensitive
- Less tolerable to M/S defects

March 2, 2011 SPIE Advanced Lithography 2011 9

Outline

- Introduction: blank quality
- Current defect status, understanding
- Defect Requirements
- **Infrastructure needs and readiness**
- Summary

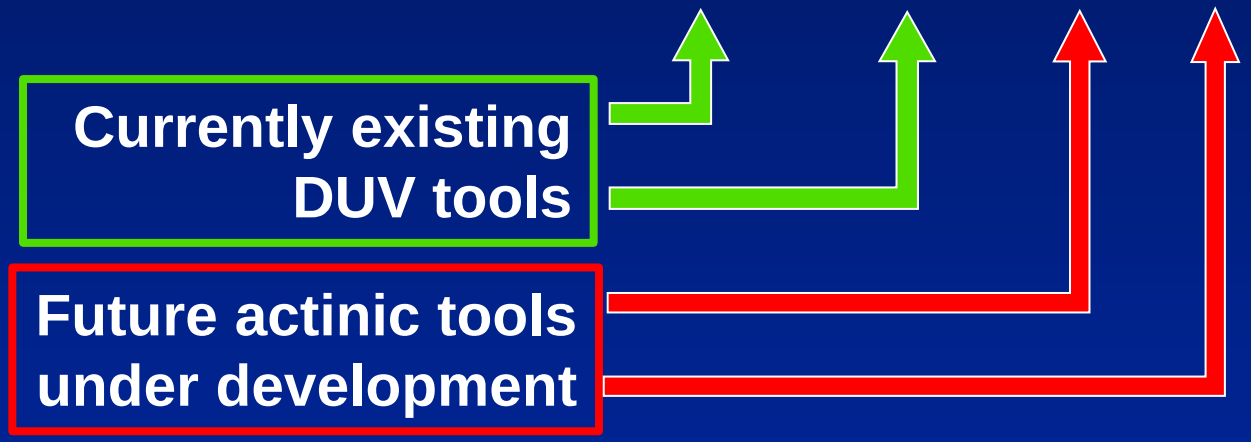
Blank Inspection Sensitivity

Well characterize test mask for tool characterization

22nm hp 16nm hp

Cell #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Surf.W	1000	750	500	300	200	180	160	140	120	100	90	80	72	66	51	43
Surf.H	1.6	1.6	1.6	1.6	1.6	1.6	1.6	1.6	1.6	1.5	1.5	1.4	1.3	1.2	1.1	1.0
SEVD	151	124	95	68	52	48	44	41	37	32	30	27	24	21	18	15

BI sensitivity assessment



- **BI tools can support pilotline and early TD learning**
- **New actinic BI development to meet the need for HVM**
  - EIDEC consortium; KLA 7XX partnership
  - Must detect amplitude defects

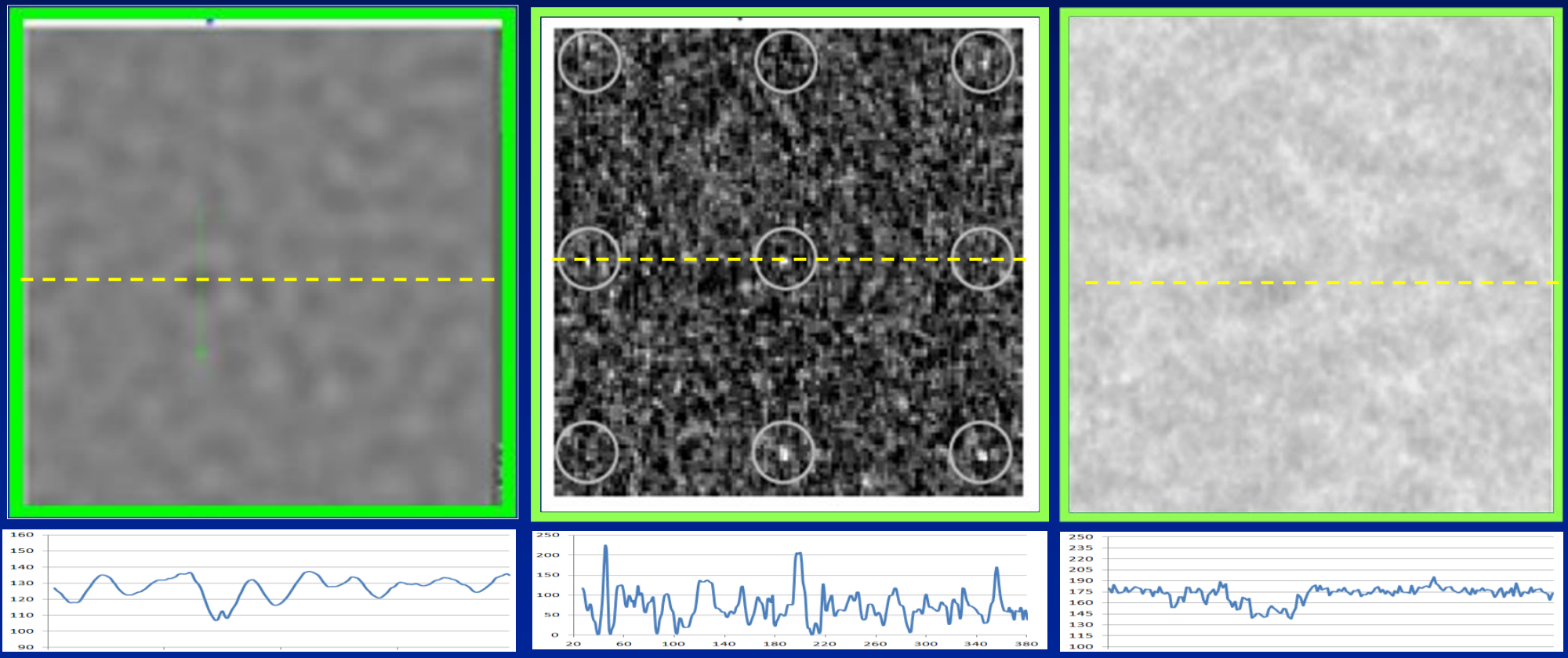
Surface Roughness Affects Inspection

- **ML roughness causes background 'noise' for inspection**

DUV optical
(# 13: 1.3nm x 72nm)

Actinic DF
(#16: 1.0nm x 43nm)

AIT
(#16: 1.0nm x 43nm)

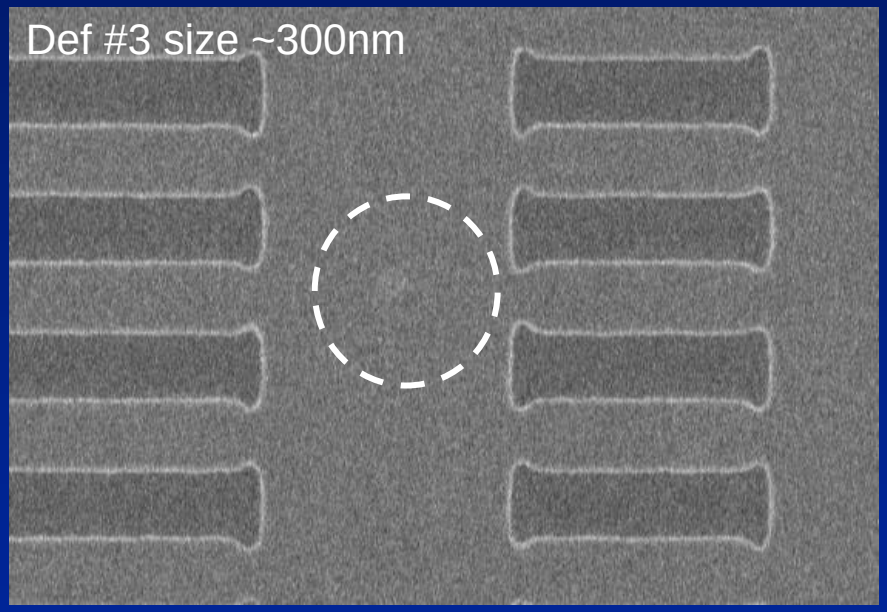


- **High frequency surface roughness must be reduced**
- **BI tool must reliably detect defects above noise floor – must not accentuate the roughness impact**

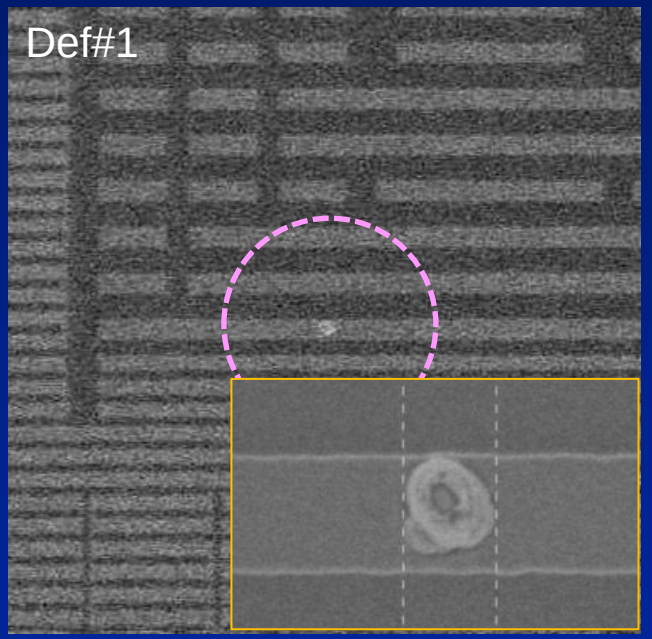
Defect Mitigation to Enable EUV Mask Yield

- Defect mitigation: adjust device pattern to 'hide' or 'avoid' ML defects (alleviate the impact to printing)
- This is necessary when blank yield is low (= cost is high) – widely recognized and tested

DF



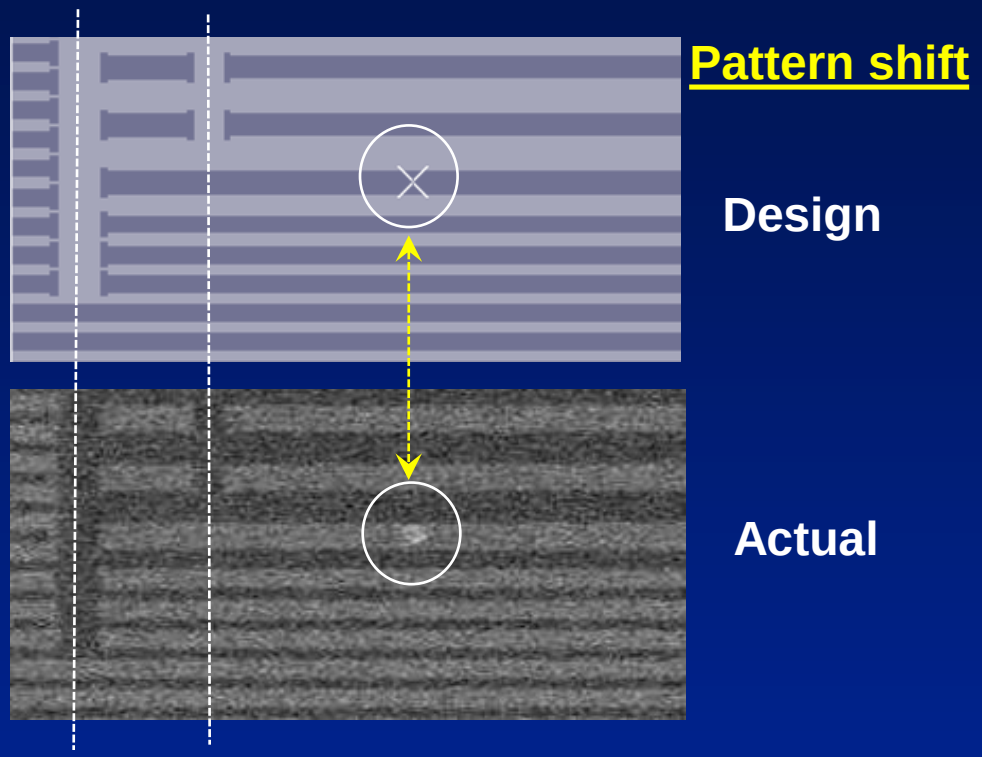
BF



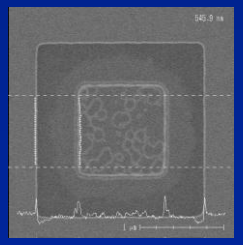
- Intel has demonstrated mitigation, powerful:
  - Dark field – cover defects by larger absorber areas
  - Bright field – Hide defects by primary patterns

Required Metrology Capability for Mitigation

- **In order for mitigation to work, defect size and location must be measured accurately**



- **Required accuracy to completely cover a 50nm defect with a 80nm mask pattern with >99% success rate**
  - Writer registration: 15nm 10nm
  - Defect location: 5nm 10nm
- **Required infrastructure**
  - Fiducials on blank
  - Location metrology : on BI tool or standalone tool
- **Benefits can be tremendous!**

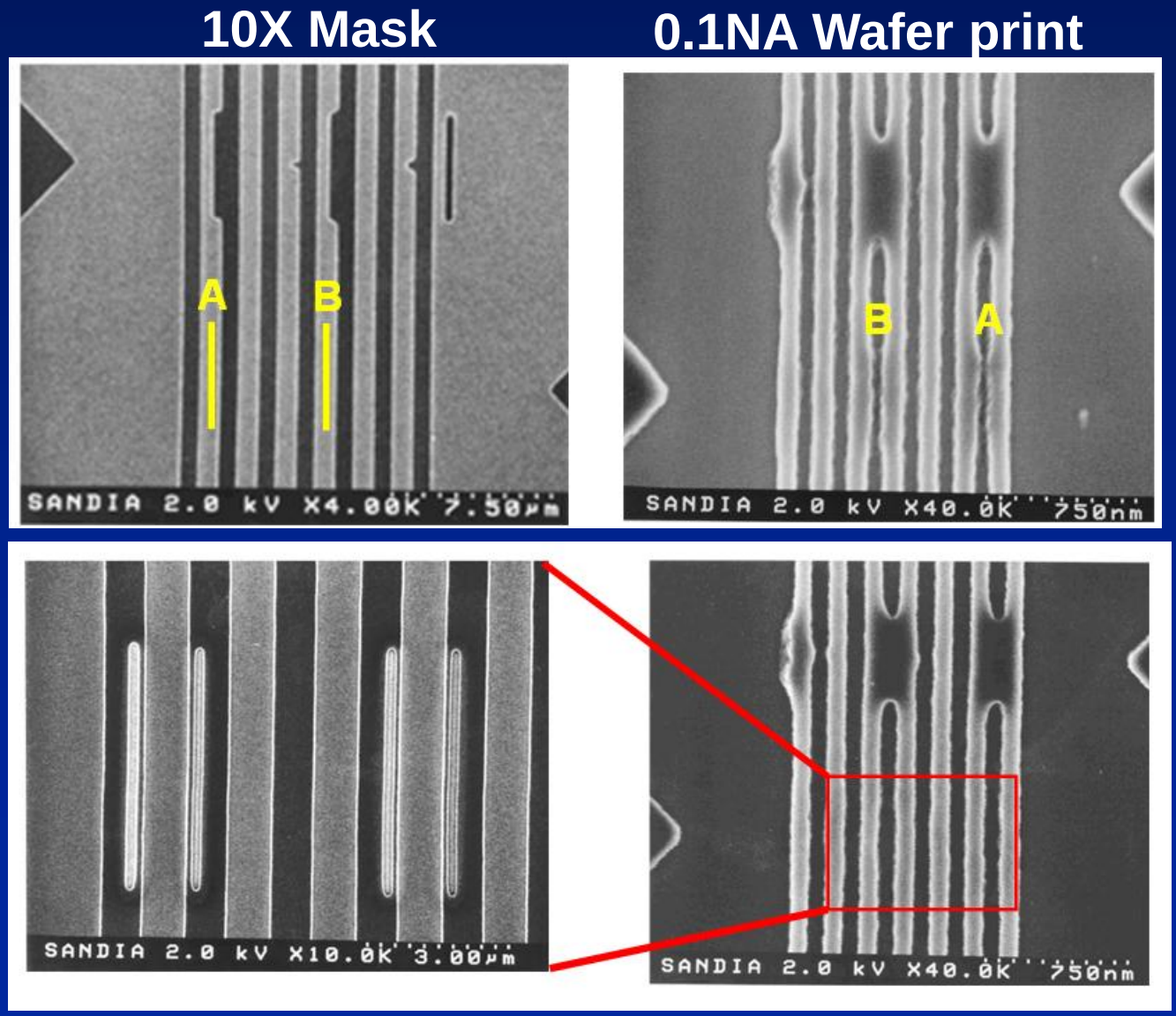


Fiducial

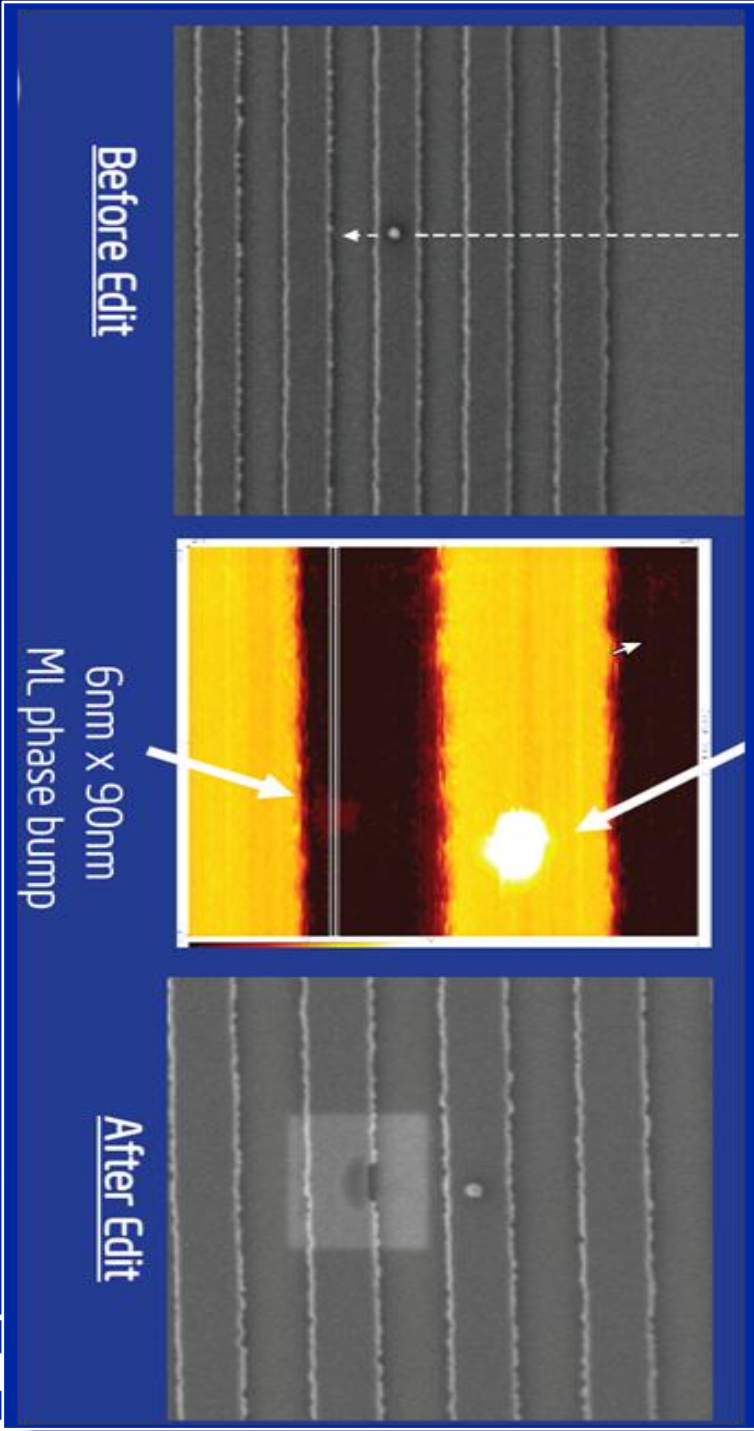
- **Achieved ~perfect overlay**
  - Δx=3.5nm
  - Δy=-1.6nm
- **High accuracy needed**

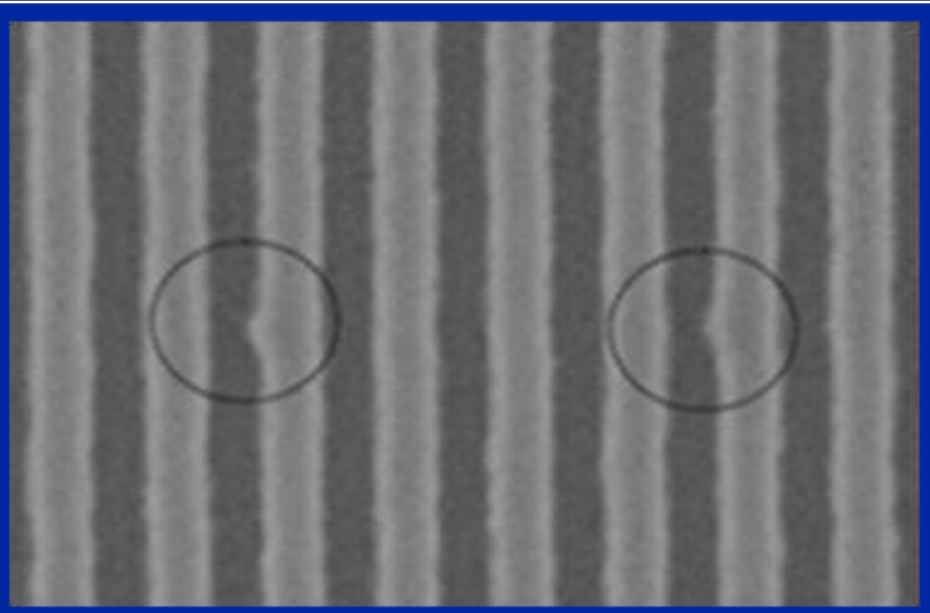
Defect Compensation Repair

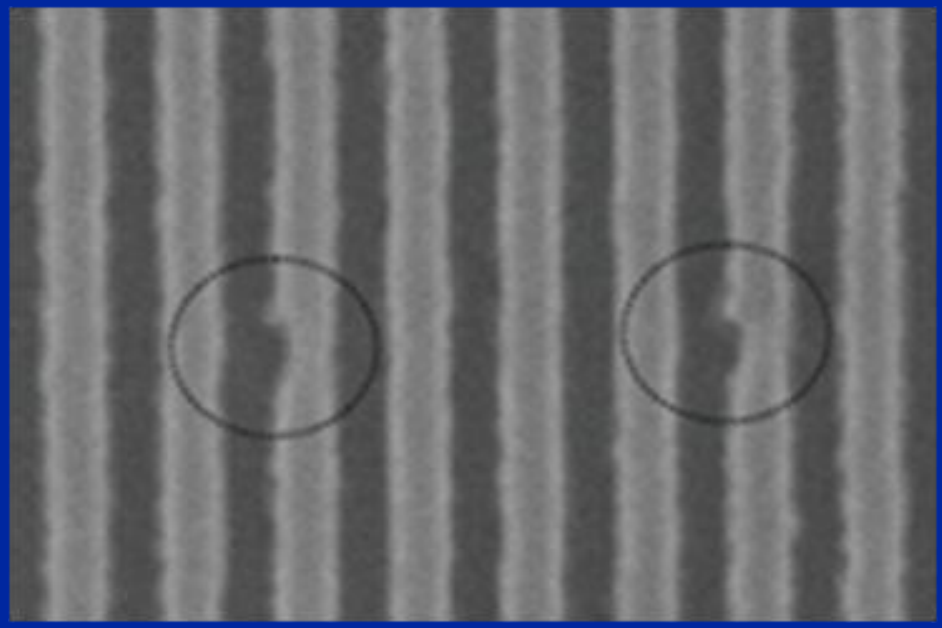
- First demonstration in 1999 with FIB (EUV LLC + VNL)
- Milling slots in the absorber to avoid ML damage by Ga-ions



Defect Compensation Repair Now







ML defect not visible
Placement slightly off

EUV AIMS for Defect Disposition

- **Wafer print for mask defect disposition is not a manufacturing solution**
  - Too slow and too expensive
- **AIMS is needed, same traditional function as for 193nm optical masks**
  - Conventional pattern defects
  - ML blank defects
  - Particles and contamination (mask re-qualification from use)
- **AIMS is also needed for ensuring the success of ML defect mitigation and compensation**
  - Feedback loop to ensure success
- **Timely delivery of AIMS tool is critical!**

Outline

- Introduction: blank quality
- Current defect status, understanding
- Defect Requirements
- Infrastructure needs and readiness
- **Summary**

Path to Readiness

- **Levels of readiness**
  - the quality of being immediate for use
    → large defect ≠ 0 yet
  - the state of being fully prepared for delivery
    → roadmap in place and know-how?!
  - willingness to do something to achieve goal
    → retain/accelerate defect reduction rate
- **Infrastructure readiness**
  - ML deposition system: free of large defects; controllable
  - Blank inspection tools: sensitive and affordable
  - Location metrology: see and locate defect accurately
  - AIMS: available on time and reliable

Summary

- **Reducing ML defects to produce quality blanks remains to be the preferred path to mask yield**
  - EUV mask fabrication = 193nm optical
- **ML defect mitigation and compensation are two essential strategies to enable mask yield until defect-free blanks become readily available**
- **Overall, the 'prognosis' looks promising in retiring the risk of mask yield being the limiter in EUVL implementation for HVM IF the key issues are addressed properly and timely**

Acknowledgements

- Intel Management for their support in committing the resources ($$$) for mask infrastructure development
- Many colleagues at Intel for their contributions
- Materials and tool suppliers, consortia partners (Sematech, IMEC) and CXRO for their collaborative efforts in working toward making EUVL a reality

Thanks for your attention